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Oxide ceramics LSI devices to mitigate global extreme weather due to computers in the AI era

SEMICONDUCTOR ENERGY LABORATORY CO., LTD.
Chairman and Chief Executive Officer
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October 9, 2025

Outline

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1. Overview ～main cause of extreme weather～
2. Homework from 45 years ago
3. Discovery of ultra-low off current
4. Advances in active displays
5. Analog AI
6. Future plans
7. Conclusion

1. Overview ～main cause of extreme weather～

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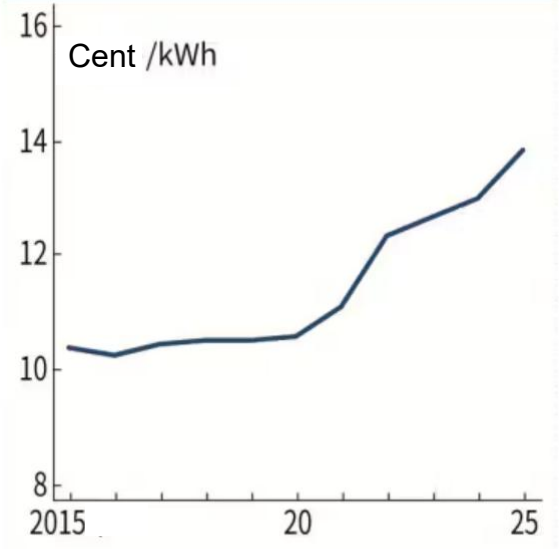
Severe global warming (including weather disaster) can be seen around the world.
Enormous power consumption of data centers for AI has influenced such climate change.

Loudoun District of Virginia known as the world's largest data center integration area.=AP

Soaring electricity prices in North America



*The price of first half of the year is marked for 2025.
Source: U.S. Energy Information Administration

Major revisions in electricity prices in US	
Dominion Energy	Announced its price increase application (basic fees and fuel fees) in Apr. and will introduce it from 2026.
National Grid	Gained regulatory approval for price increase in August and will increase the price by $14 per month for a standard household from Sep.
APS	Applied for price increase in June, requesting increase of $20 per month for a standard household.
AEP Ohio	Introduced DC-dedicated menu and requested to take measures against unnecessary possession of the transmission and distribution network and to cover the costs associated with withdrawal.

The Nikkei dated Sep. 20, 2025
https://www.nikkei.com/nkd/company/us/D/news/?DisplayType=1&ng=DGKKZO91431700190920 25EA5000

Reduce power consumption of data center to 1/100

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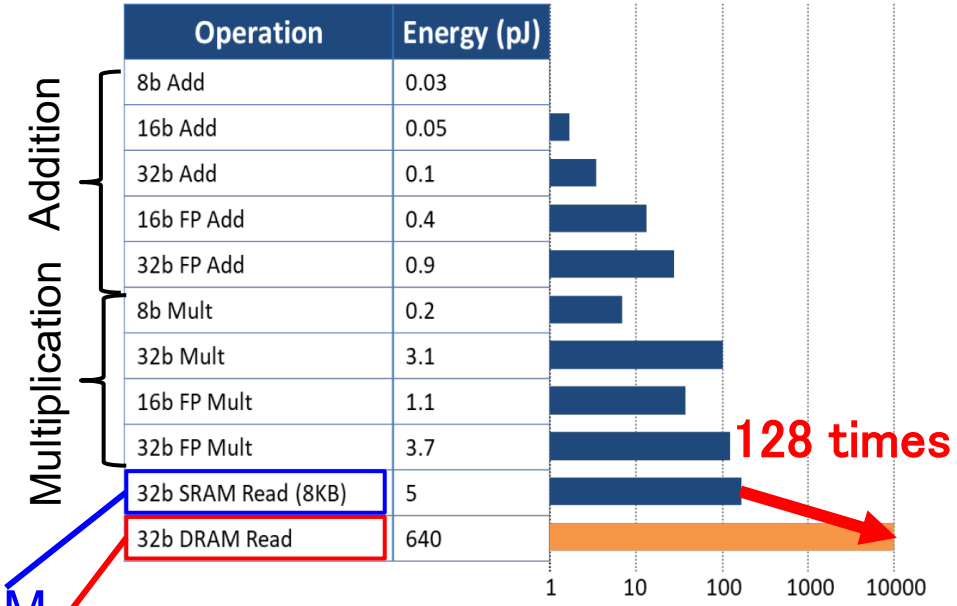
1) In recent years, server power consumption has increased.
   - Power for multiply-accumulate (MAC) operation
   - Power for operation other than MAC operation (data transfer)

2) Memory, especially DRAM, has high power consumption.

3) Both shall be shown in this presentation.

Relative comparison of energy



Comparison of digital computation energy
(Excerpt from ISSCC2025 F3.4, with additional notes)

Reduce power consumption of data center to 1/100

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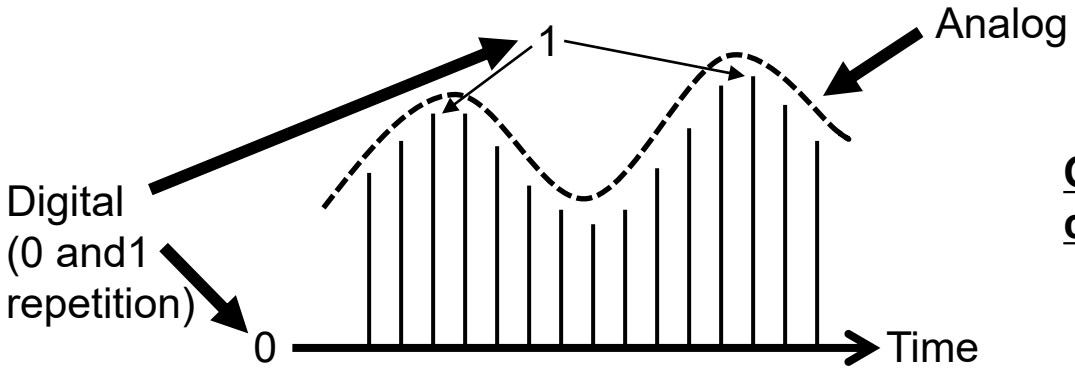
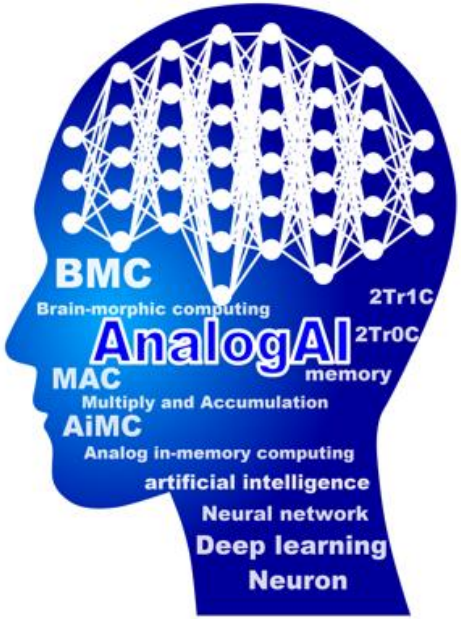
To achieve 1/100 of the current power consumption of digital AI data centers, the following concepts can be the solutions.

1) 3D stack of MAC (multiply-accumulate cells) and oxide memory system using Crystal IO FET (high μ and ultra-low off current)
2) Change from digital AI to analog AI





Our target is making existing devices close to the human brain.

New AI age may be coming.

Ref) Crystal IO: Pat No. JP7538371, US12225739

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Where did these concepts come from?

1) Homework given 45 years ago in 1980 by Dr. R. N. Noyce
   "Create a flash memory that does not degrade"
2) Discovery of ultra-low off current of 10^{-21} (zepto) to 10^{-24} (yocto) A/μm (RT) using oxide semiconductors, especially Crystal IO

These concepts for ultra-low power consumption came from the "combination" of 1) and 2).

2. Homework from 45 years ago

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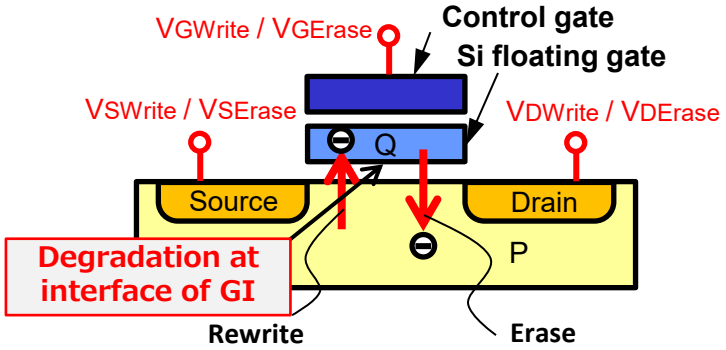
Commercialized non-volatile memory (flash memory) has a write/erase operation limit of only $<10^4$ times.



The basic device of silicon flash memory was invented by me at the age of 28.

Japanese Examined Patent Publication No. S50-36955
(filed on Oct. 27, 1970, Japanese Patent Application Serial No. S45-94482)
Japanese Patent No. 886343

Dr. R. N. Noyce, the founder of Intel, gave me a homework in 1980
"Create a flash memory that does not degrade".

Lecture at ECS Washington Meeting was covered by News Paper. (Mainichi News paper, Shizuoka edition, on May 31, 1971)


すばらしい研究だ
米国で世界の学者称賛
"若い学徒"の成果に驚く
シリコントランジスタの山崎博士

Before lecture at ECS Washington Meeting in May 1971

Ref) Japanese Examined Patent Publication No. S49-22356, S50-1986, S50-36955

Non-volatile memory device Yamazaki created in about 1971 (54 years ago)

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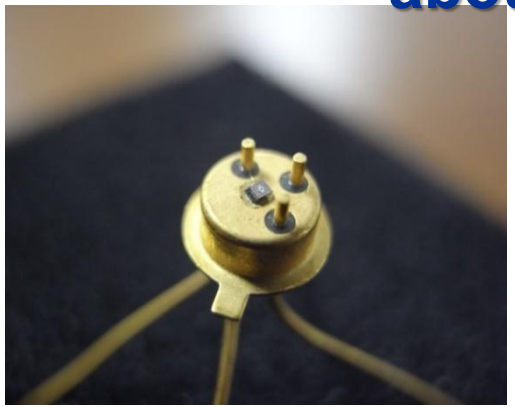
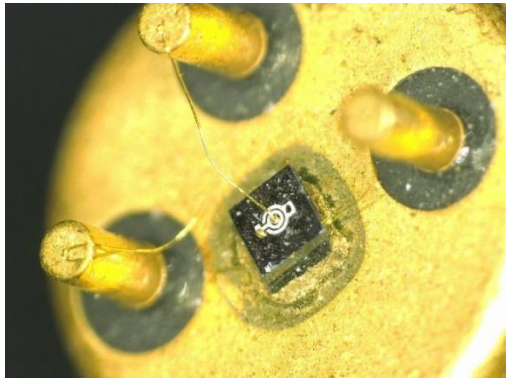
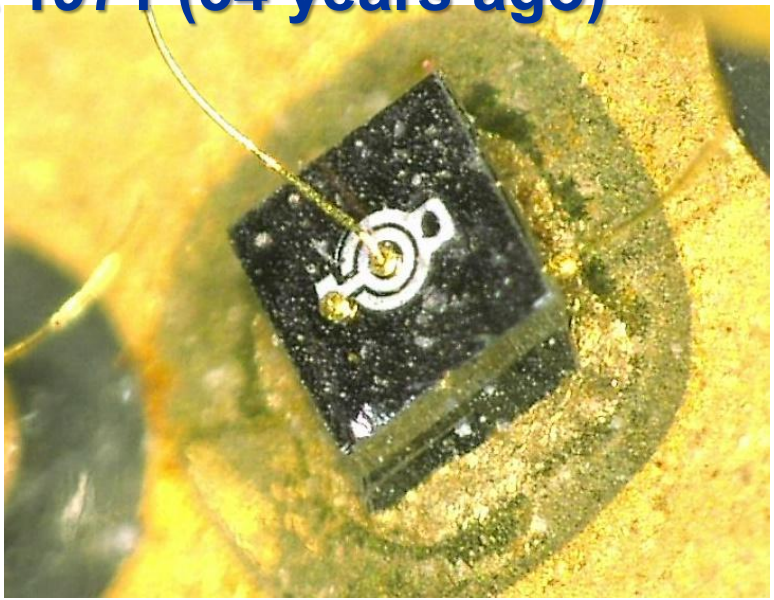


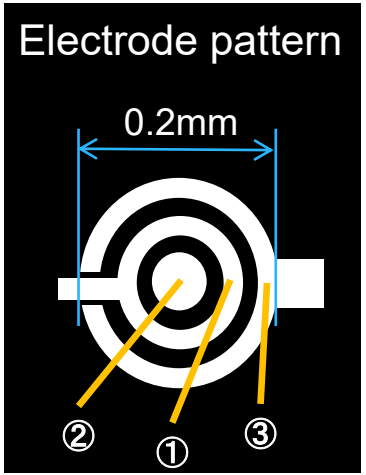




Enlarged photo of device

Still good driving

Flash memory



① is the gate.
One of ② and ③ is the source, and the other is the drain.

Application of oxide semiconductor to memory

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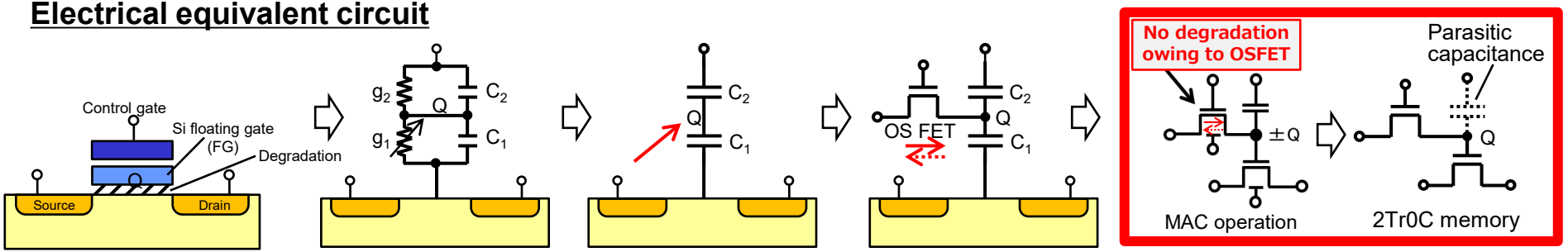
A method using tunnel current causes “degradation of the interface of FG and insulator (decrease in memory window and write speed)” due to injection by a strong electric field.

→To create a floating gate that does not degrade.

Electrical equivalent circuit



g1 tunnel current conductance
At high voltage, current flows.
At low voltage, current does not flow.
Cause of degradation.

Detect g1 and g2. However, how can we put Q into the floating gate?

OSFET has extremely low off current and functions in the same way as tunnel current with no degradation.

Achieved using Crystal IO with high on current and extremely low off current

If parasitic capacitance is enough, 2Tr0C may be used.

Ref) Pat No. 886343

3. Discovery of ultra-low off current (2012)

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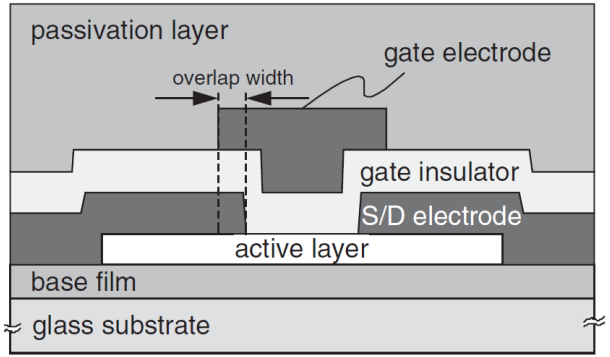
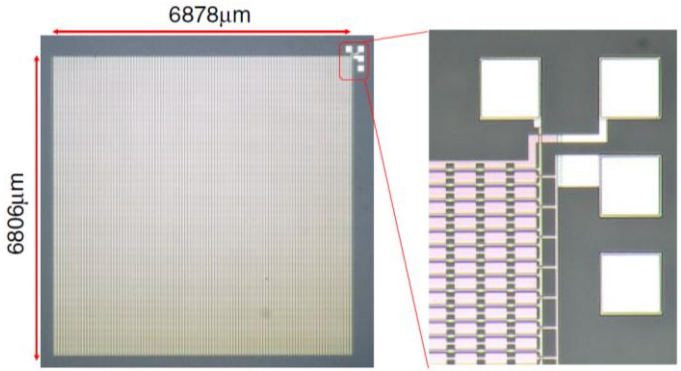
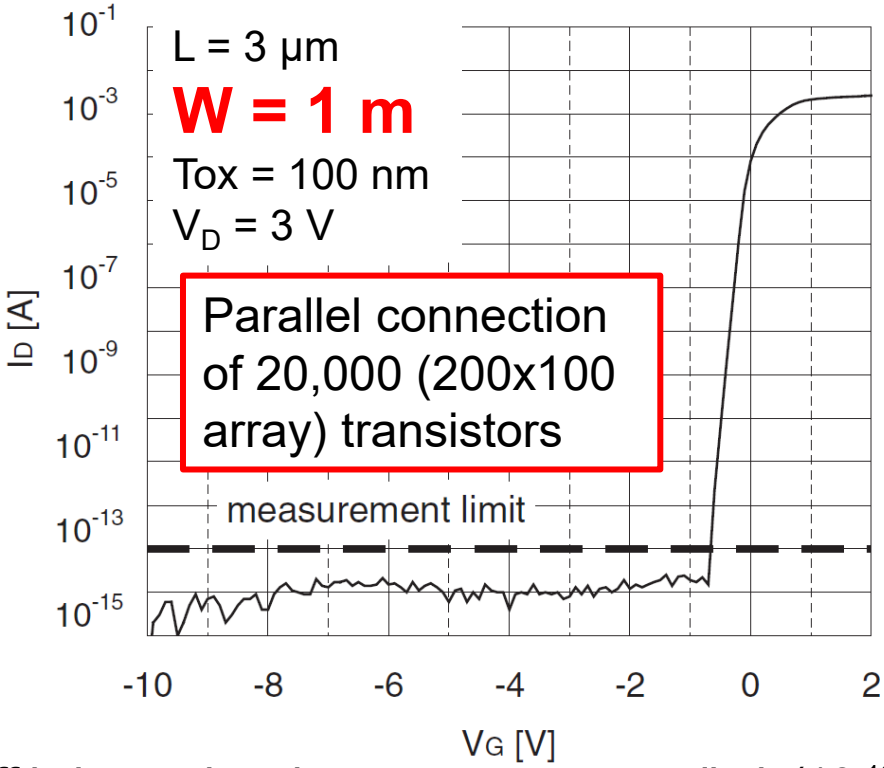




* K. Kato, J. Koyama, S. Yamazaki *et al.* Japanese Journal of Applied Physics 51 021201-01 (2012)



Ioff is lower than lower measurement limit (10^{-13} A at RT) even when W is as huge as 1 m.

Ref) Ioff：Pat No.JP6773823、US9553583

Ultra-low Ioff characteristics and Ion (high mobility) of Crystal IO

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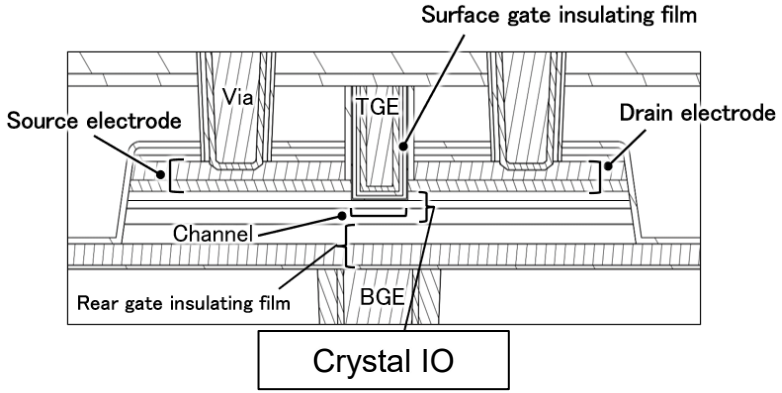
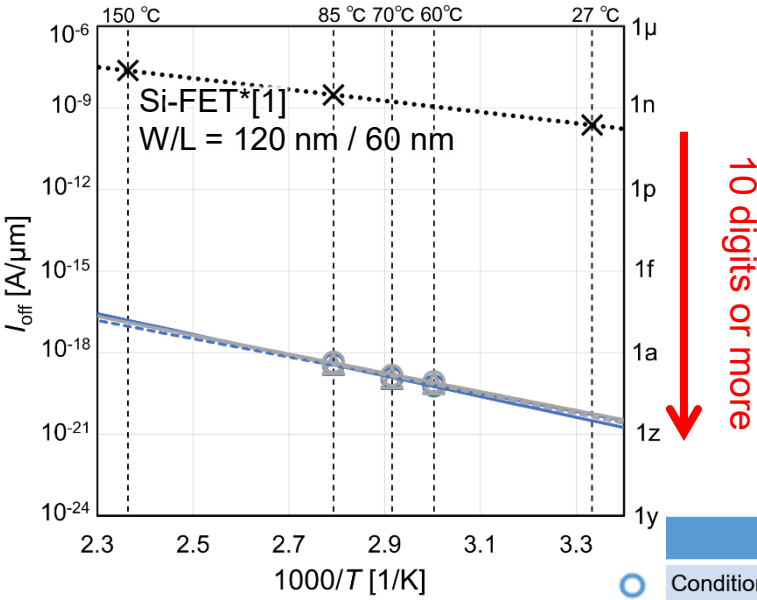
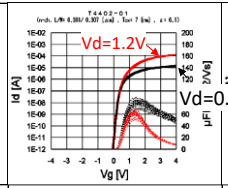
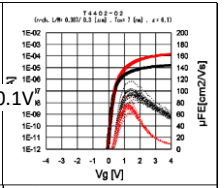


Measurement TEG: L/W = 360 nm / 360 nm
Parallel-connected transistors: 90000



Top gate driving (Vbg = 0 V) L/W = 360 nm / 360 nm (design)			
μFE①(Vd=0.1V)	X̄:(Median) [cm2/Vs]	80.2	< 95.2
Ion(Vg=Vsh+2.5V)	X̄:(Median) [μA]	65.3	< 73.6
S.S.(Vd=1.2V)	X̄:(Median) [mV/dec]	71.5	71.9
Vsh(Vd=1.2V)	X̄:(Median) [V]	-0.04	> -0.09
	σ(Variation) [mV]	23.9	48.1
Vth(Vd=1.2V)	X̄:(Median) [V]	0.15	0.11
	σ(Variation) [mV]	26.2	47.3

*Measurement conditions: Vtg or Vbg = -4 V to +4 V, 0.1 V step, Vd = +0.1 V, +1.2 V, Vs = 0 V, Keysight Technologies semiconductor parameter analyzer
*Measurement results of μFE at Vd = 0.1 V, measurement results of S.S, Vsh, and Vth at Vd = 1.2 V, and measurement results of Ion at Vd = 1.2 V and Vg = Vsh + 2.5 V are shown here.

	85℃, Ioff
○ Condition1-1	1.34E-19 [A]
△ Condition1-2	1.32E-19 [A]
○ Condition2-1	1.59E-19 [A]
△ Condition2-2	1.42E-19 [A]

Ref) H. Kunitake *et al.*, SSDM, pp. 787–788, 2018.
Dhananjay, Chu C.-W. APPLIED PHYSICS LETTERS 91, 132111 (2007).
Yamazaki S. and Godo H. (2011). US patent 9,209,092. (JP patent 6,843,279)

4. Advances in active displays (2012-)

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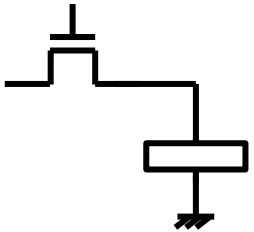
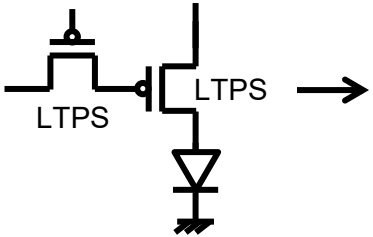
2012-



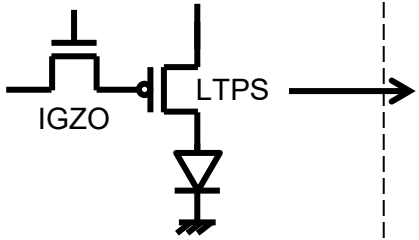
IGZO
LCD

2013-



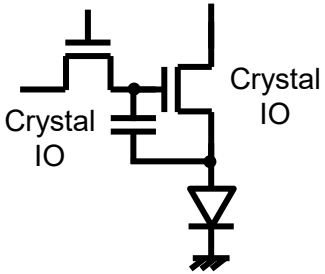
LTPS (smartphone)
OEL (high quality)

2021-



LTPO (smartphone)
OEL (higher quality and power saving)

Coming soon

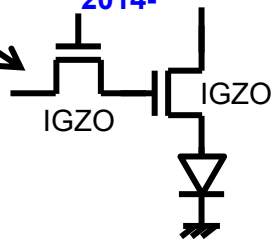


OEL
Crystal IO
(TV, smartphone, vehicle display)

Simple back plane, high quality, and power saving

World's first mass production of a product using CAAC-IGZO

2014-



IGZO (TV)
OEL (power saving)

Displays also use "analog 2Tr1C structure".
SEL is leading advances in the industry.

Time

Ref) Y. Kataoka et al., SID 2013, 56.1
Ref) LTPO : Pat No. JP7554334, US12027528

8K-OLED crystal IO display

8.3 inch, Ultra high definition 8K crystal IO panel

5. Analog AI

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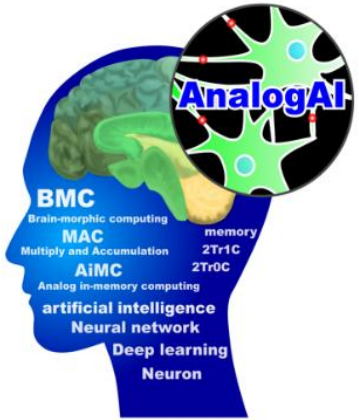
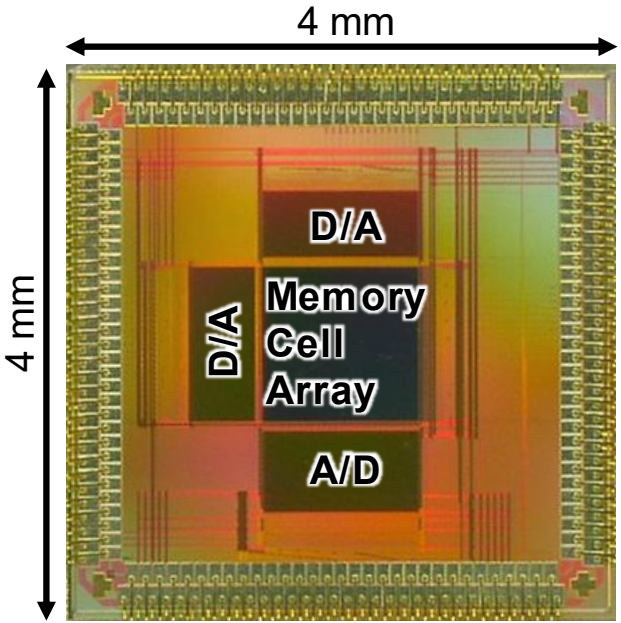
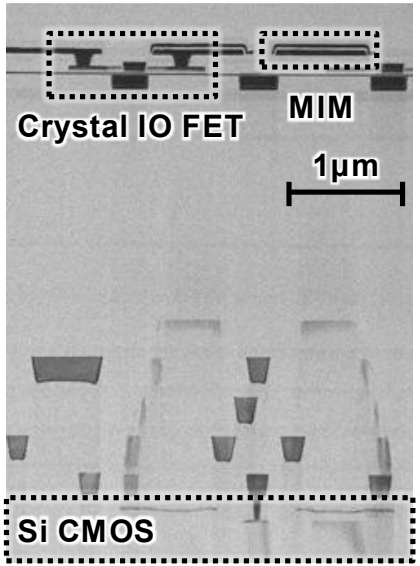


1) AiMC using Crystal IO FET



Chip micrograph



Cross-sectional STEM image

- Crystal IO can achieve both high Ion and ultra-low Ioff
- Sub th (subthreshold) region of Crystal IO FET with GL structure is utilized

Consider multi-layered cell array
Demonstrate 3 layered 3D structure
Lots are in process

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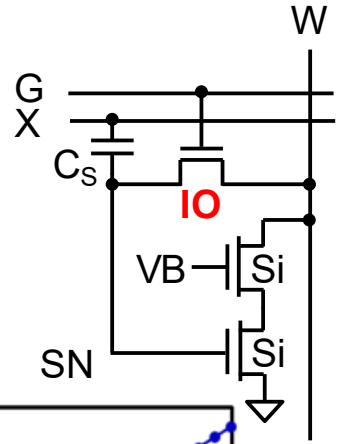
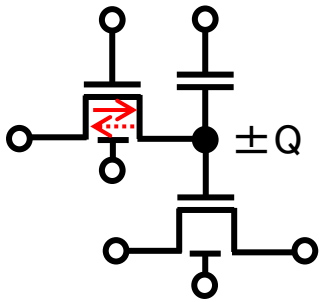
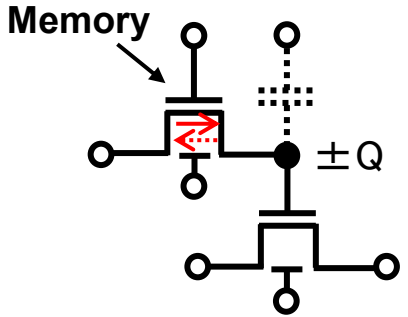
2) MAC (multiply-accumulate) using Ioff (fA)



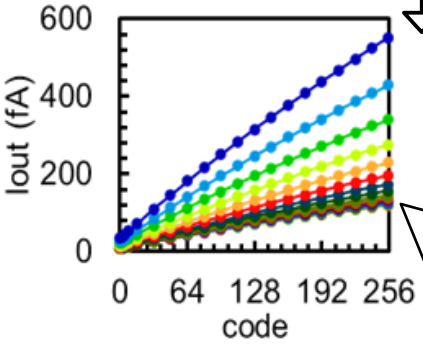


(2Tr1C)

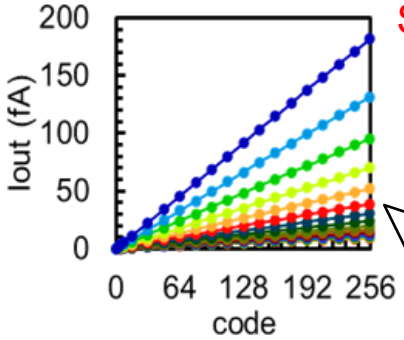


2Tr0C

Same equivalent circuit as flash memory



Si cells cannot output correctly with small current.



IO cells can output correctly with extremely small current.
➡Lower power loss

Unit Prefix

femto	(10^{-15})
atto	(10^{-18})
zepto	(10^{-21})
yocto	(10^{-24})

MAC current (sub th **0.4a to 100fA**) is used.

Ref) 2Tr0C : JP6743315, US10490553, 3Tr0C : JP7628157, US12205622
Kazuki Tsuda et al., J. Electron Devices Soc., 12, 594-604 (2024).

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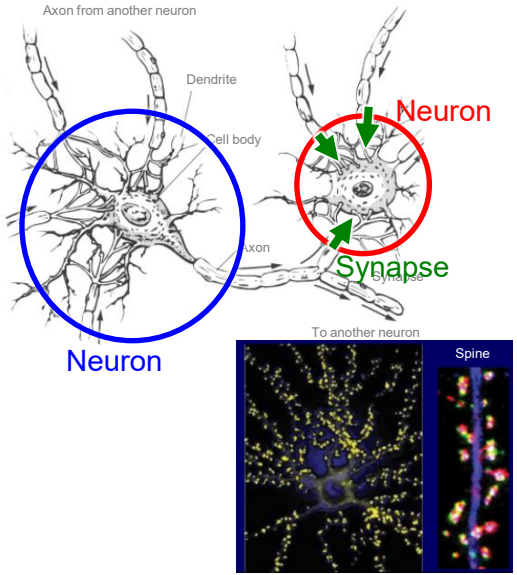
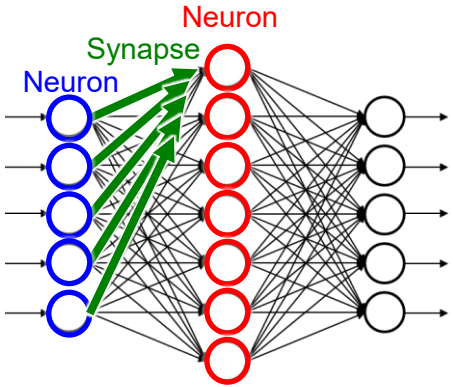
3) Analog neural network

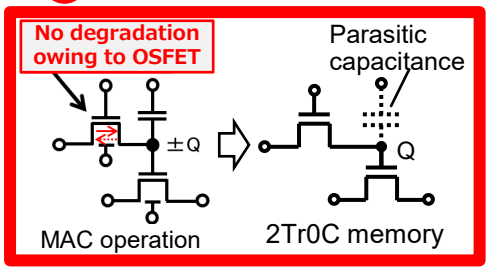
Neural networks imitate neurons of nerve cells, and we implement their function as an analog circuit.

Neurons

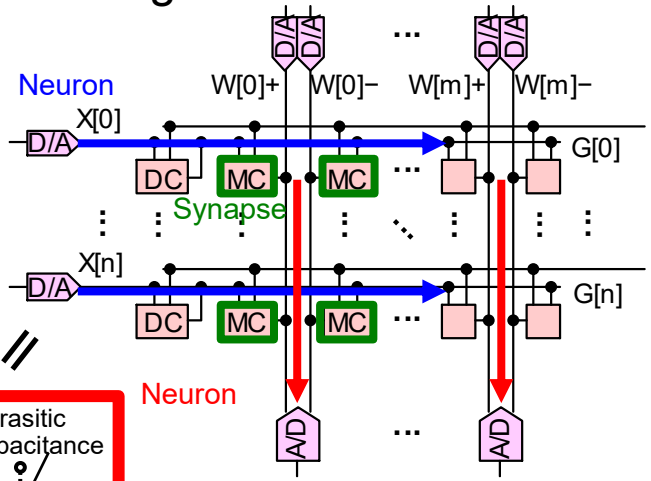


Neural Network



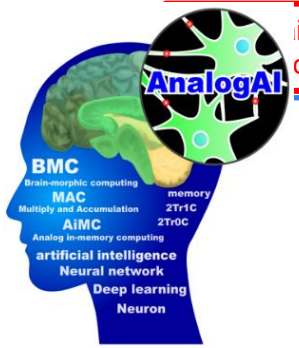


Analog Neural Network Circuit



MC : Memory cell
DC : Driver cell
A/D : Analog to digital
D/A : Digital to analog

Ref) T. Aoki et al., Ext. Abstr. Solid State Devices and Materials, 191 (2017)



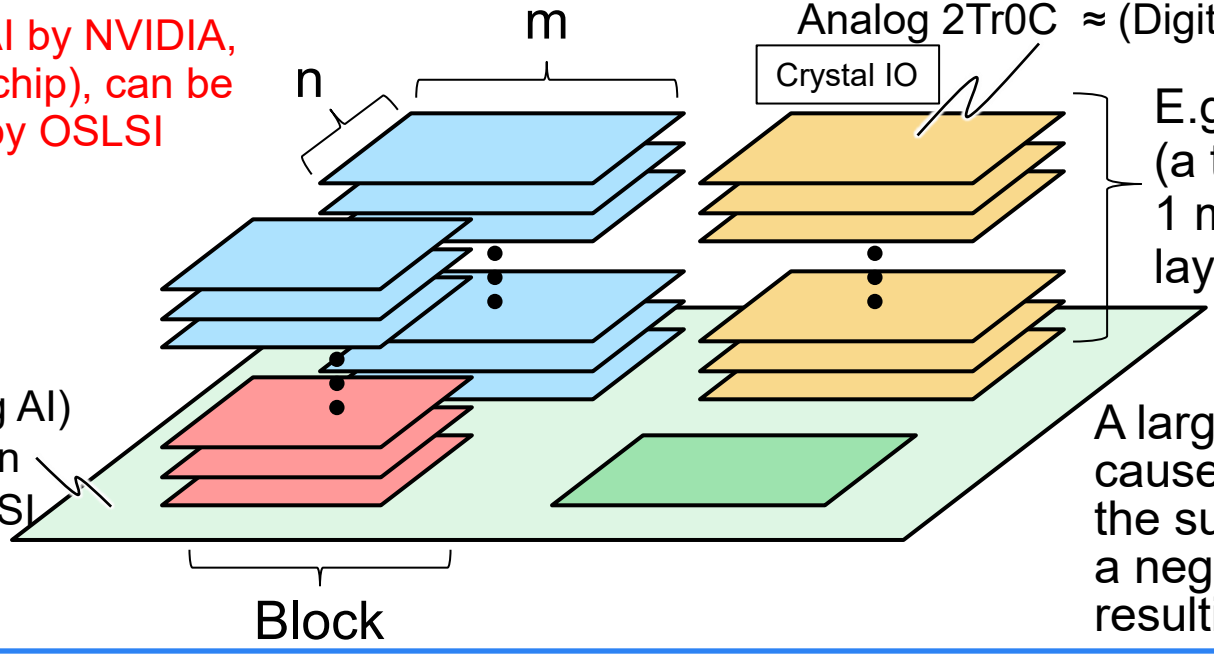
4) Brain-morphic computing (in verification process)

300 layers × m × n × 3 bits (8 values) × the number of blocks

Latest digital AI by NVIDIA, H200 (600 W/chip), can be two digit less by OSLSI

NOSRAM

Analog 2Tr0C ≈ (Digital SRAM + DRAM)



A larger thickness will cause the stress on the substrate to have a negative impact, resulting in defects

6. Future plans

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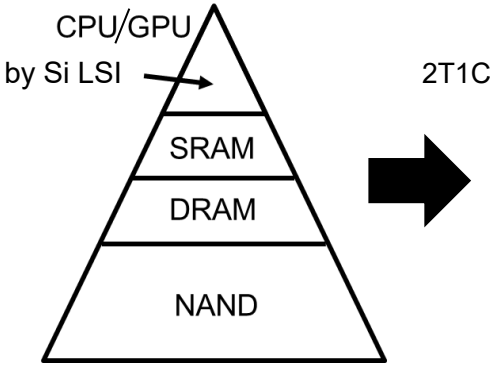
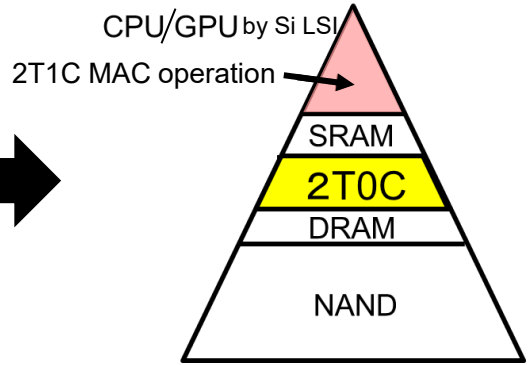
1) We aim to deny DRAM whose power consumption is large.
   ⇒ For this, we will achieve high-speed MAC operation with a 3D stack structure of MAC and memory using the sub th (subthreshold) current of Crystal IO FETs.
2) The invention of the Si floating gate/flash memory in 1971 has evolved into analog AI over 54 years, offering the prospect of significant reductions in the power consumption of data centers.

Present digital memory hierarchy

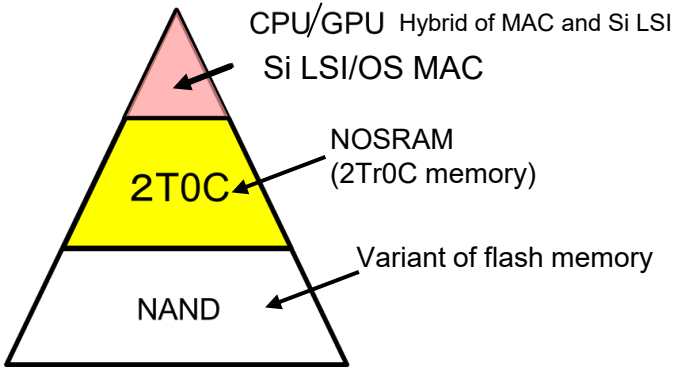


Short-term goal



Medium- and long-term goals

No DRAM use and 1/100 power consumption



MAC: Multiply-accumulate

Application examples of AiMC and analog AI

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Analog AI
AiMC＼3D 2Tr0C memory

Exterior photo of a robot for analog AI demonstration purpose

Robot size：
Height：401 mm
Width：194 mm
Length：129 mm

Small-scale use of AI

Exterior photo of AI-SPC SEL's data center (DC) with 100 units of H200 (Power consumption: 152.4 kW (maximum))

Large-scale use of AI

Ref) Shunpei Yamazaki et al., Int. J. Ceram. Eng. Sci., 7(4), e70011 (2025).
Ref) Nathan Leroux, et al. Nature Computational Science 5, 813-824 (2025).

7. Conclusion

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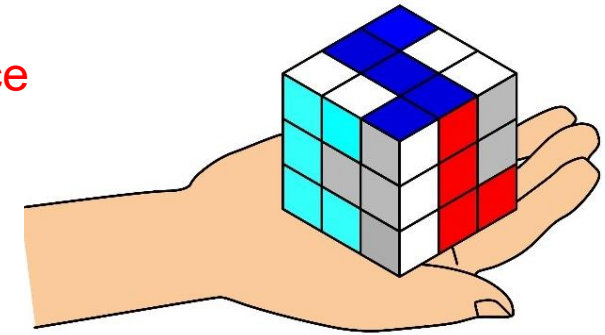
1) AI will shift from digital AI to analog AI using oxide semiconductors, especially Crystal IO.

2) Compared to the latest AI LSIs, NVIDIA B200 and H200, the power consumption is approximately 1/10 and the memory capacity is about 10 times larger according to our calculations. The calculations also show that the power consumption can be reduced (and the efficiency can be increased) by two digits. It's not impossible in future that a data center may be on a hand like a cube.

3) To put the brakes on global boiling, analog AI can reduce power consumption to 1/100 or less.



4) Having heard this, an expert was excited and commented:
“This technology can save the earth”.

Finally…

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I invented the flash memory about 55 years ago (in 1971) and have been conducting R&D on OSLSI technology for nearly 20 years.
I believe that combining the discovery of ultra-low off current with 2Tr1C and 2Tr0C technology can “stop the global boiling”.
The time has come for Crystal IO, a ceramic material, to bring about a significant transformation in the display and LSI fields.

I am deeply grateful for the homework from 45 years ago.

Thank you for your attention.

SEL
SEMICONDUCTOR ENERGY LABORATORY

Achievements

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■ Figures of flash memory*1)

Market figures (shipment value) of USB*2) memory (USB flash drives) in 2020

- USB memory: 7.96 billion USD (≈ 850 billion JPY*3))

■ Figures of OS display*2)

Market figures (shipment value) of OS displays using IGZO from 2020 to 2021

- LCD (Oxide): 18.0 billion USD (≈ 1.9 trillion JPY*3))
- OLED (LTPO): 10.6 billion USD (≈ 1.1 trillion JPY*3))

*1) Cited from documents created by Emergen Research
*2) USB: Universal Serial Bus
*3) Calculated at 1 USD = 106.94 JPY (2020 average exchange rate)
*4) Cited from documents created by OMDIA

References (1)

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SEL Patents

■ Flash memory

S. Yamazaki (1970). JP patent 761,848.
S. Yamazaki (1971). JP patent 813,295.
S. Yamazaki and Y. Sugimura (1970). JP patent 886,343.
S. Yamazaki et al. (1971). JP patent 957,839.
S. Yamazaki (1971). JP patent 1,105,278.

■ FET structure

2Tr0C: S. Yamazaki et al. (2009). JP patent 6,743,315.
S. Yamazaki (2009). US patent 10,490,553.
2Tr0C: S. Yamazaki et al. (2009). US patent 9,135,958. (JP patent 6,978,473)
2Tr1C: S. Yamazaki et al. (2009). US patent 9,054,201. (JP patent 5,577,230)
LTPO: K. Takahashi and S. Yamazaki (2009). JP patent 7,554,334.
K. Takahashi and H. Miyake (2016). US patent 12,027,528.

References (2)

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■IGZO/IO (Indium Oxide)/MAC (Multiply-Accumulate)

IGZO (CAAC): S. Yamazaki et al. (2009). US patent 9,935,202. (JP patent 5,172,918)

IGZO (Ioff): S. Yamazaki et al. (2009). US patent 9,478,564. (JP patent 6,697,066)

IO: T. Honda et al. (2011). US patent 12,225,739. (JP patent 7,538,371)

MAC: T. Ikeda and Y. Kurokawa (2015). US patent 10,699,794. (JP patent 6,192,798)

SEL books

N. Kimizuka and S. Yamazaki, Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Fundamentals, Wiley, (2017).

S. Yamazaki and M. Fujita, Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to LSI, Wiley, (2017).

S. Yamazaki and T. Tsutsui, Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to Displays, Wiley, (2017).

References (3)

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IGZO (Ioff): K. Kato, J. Koyama, S. Yamazaki et al., Jpn. J. Appl. Phys., 51, 021201-01 (2012)
*ANN[*1)]: T. Aoki et al., Ext. Abstr. Solid State Devices and Materials, 191 (2017)
*IGZO (2Tr1C): S. Yamazaki et al., Int. J. Ceram. Eng. Sci., 1(1), 6 (2019)
*AiMC[*2)]: K. Tsuda et al., J. Electron Devices Soc., 12, 594 (2024)
*Analog AI[*3)]: S. Yamazaki et al., Int. J. Ceram. Eng. Sci., 7(4), e70011 (2025)

Others' papers

IO: Dhananjay, Chu C.-W., Appl. Phys. Lett., 91, 132111 (2007)
*AiMC: L. Fick et al., Proc. Cust. Integr. Circuits Conf., 17-4 (2017)
*Analog AI: J. Welser et al., IEDM Tech. Dig., 21 (2018)
*AiMC: N. Leroux et al., Nat. Comput. Sci., 5, 813（2025)

Our review reveals that the keywords "ANN", "AiMC", and "Analog AI" used in prior research have roughly the same meaning.

*1) ANN: Analog neural network, *2) AiMC: Analog in-memory computing, *3) Analog AI: Analog artificial intelligence

SEL's granted JP/US patents in all OS*1)-related areas 2)

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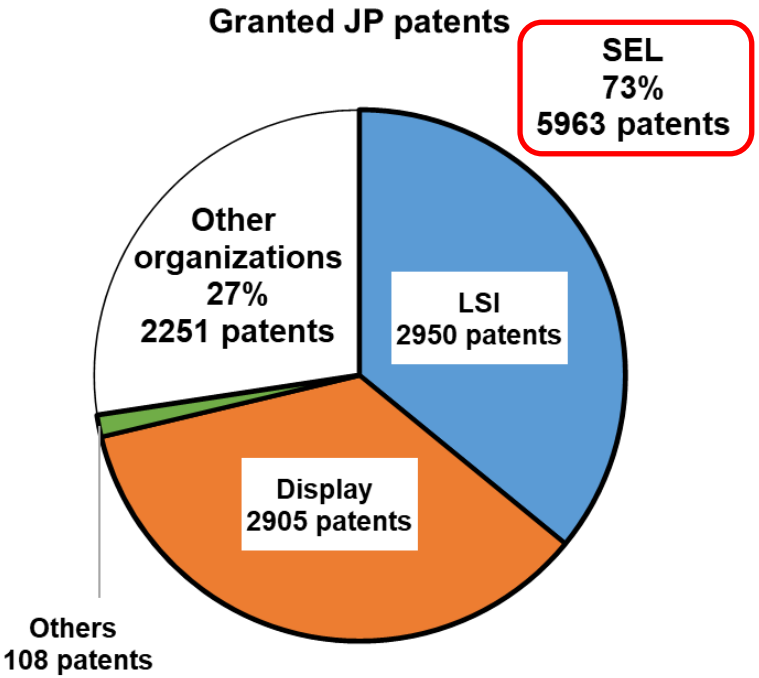

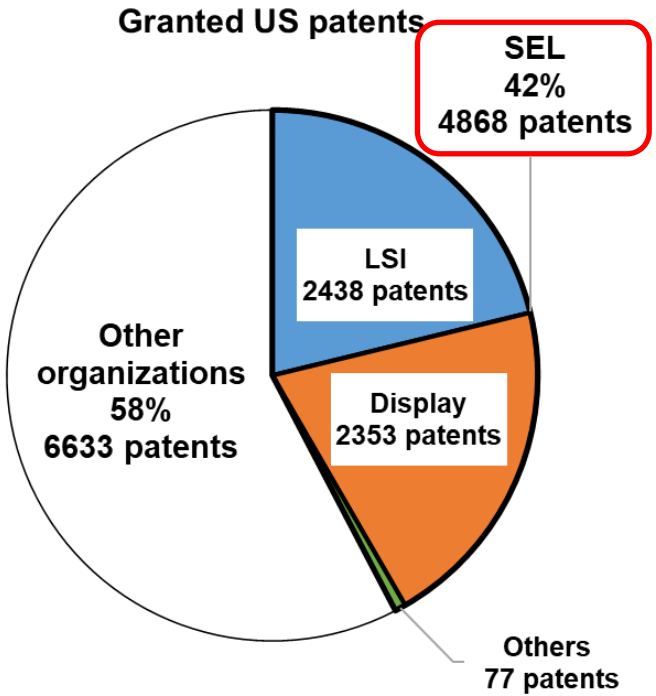

SEL has historically been conducting R&D for a long time and has large shares of granted JP and US patents in all areas of oxide semiconductors.

*1) OS: Oxide Semiconductor, *2) As of 9/30/2025